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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 09/839,963 04/23/01

Sangki Hong, Subhash Gupta,
Paul Kwok Keung Ho

A METHOD TO FORM SELF-ALIGNED
ANTI-VIA INTERCONNECTS

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,512,514 to Lee, "Self-Aligned Via and Contact Interconnect Manufacturing Method", teaches a method to form an integral via and contact interconnect.

U.S. Patent 5,693,568 to Liu et al., "Reverse Damascene Via Structures", discloses a method to form reverse damascene interconnects.

U.S. Patent 4,917,759 to Fisher et al., "Method for Forming Self-Aligned Vias in Multi-Level Metal Integrated Circuits", teaches a method to form self-aligned vias.

U.S. Patent 5,861,673 to Yoo et al., "Method for Forming Vias in Multi-Level Integrated Circuits, for Use with Multi-Level Metallizations", teaches a method to extend the surface area of a metal region wherein a via contact is planned.

U.S. Patent 5,846,876 to Bandyopadhyay et al., "Integrated Circuit Which Uses a Damascene Process for Producing Staggered Interconnect Lines", discloses a method to form damascene interconnects with staggered levels.

U.S. Patent 5,691,238 to Avanzino et al., "Subtractive Dual Damascene", teaches a reverse damascene method.

Sincerely,

George O. Saile

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